What is claimed is:

1. An inverter circuit comprising:

a switching device operable to perform a switching operation corresponding to a gate control signal input to a gate terminal, convert an input direct current to an alternating current, and output the alternating current;

an HVIC operable to input the gate control signal to the gate terminal of the switching device;

a controller operable to input to the HVIC a control signal for enabling the HVIC to generate the gate control signal; and

an impedance cell located between the HVIC and one terminal of the switching device operable to reduce voltage drop of the HVIC.

2. The circuit of claim 1, wherein the switching device comprises an insulated gate bipolar transistor having a collector terminal and an emitter terminal, wherein the collector terminal is coupled to a direct current input power source and emitter terminal is connected to an output terminal.

3. The circuit of claim 2, wherein the impedance cell is located between the HVIC and the emitter terminal of the insulated gate bipolar transistor.

4. The circuit of claim 1, wherein the switching device comprises an MOS field effect transistor having a drain terminal and a source terminal, wherein the drain terminal is connected to a direct current input power source and the source terminal is coupled to an output terminal.

5. The circuit of claim 4, wherein the impedance cell is disposed between the HVIC and the source terminal of the MOS field effect transistor.

6. The circuit of claim 1, further comprising a bootstrap circuit operable to transmit energy to a high-side region of the HVIC.

7. The circuit of claim 6, wherein the bootstrap circuit comprises:

a power source;

a bootstrap resistor connected in series to the power source;

a bootstrap diode having an anode terminal connected in series to the bootstrap resistor and having a cathode terminal opposite the anode terminal; and

a bootstrap capacitor connected to both the cathode terminal of the bootstrap diode and a node that is commonly connected to the HVIC and the impedance cell.

8. The circuit of claim 1, wherein the impedance cell comprises a resistor.

9. The circuit of claim 1, wherein the impedance cell comprises a resistor and a diode connected in parallel.

10. The circuit of claim 9, wherein the diode is located such that an anode terminal of the diode is connected to the switching device and a cathode terminal of the diode is connected to the HVIC.

11. The circuit of claim 9, wherein the diode is located such that the anode terminal of the diode is connected to the HVIC and the cathode terminal of the diode is connected to the switching device.

12. The circuit of claim 1, wherein the impedance cell comprises a first resistor, a second resistor connected to the first resistor in parallel, and a diode connected to the first resistor in parallel and to the second resistor in series.

13. The circuit of claim 12, wherein the diode is located such that an anode terminal of the diode is connected to the switching device and a cathode terminal of the diode is connected to the HVIC through the second resistor.

14. The circuit of claim 12, wherein the diode is located such that the anode terminal of the diode is connected to the HVIC through the second resistor and the cathode terminal of the diode is connected to the switching device.